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(54) Title: GAS DISCHARGE DISPLAY AND METHOD FOR PRODUCING SUCH A DISPLAY

(57) Abstract

A gas discharge display and the method of making same utilizing integrated circuit fabrication techniques. The display is manufactured from heat and pressure resistant planar substrates (200, 212) in which cavities (208) are etched, by integrated circuit manufacturing techniques, so as to provide individual pixels. Orthogonal electrodes (202, 214) are deposited on the substrates and extend into the cavities. The cavities are filled with gas discharge materials, such as plasma, upon energization of the electrodes the individual cavities forming the pixels may be individually activated.

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Gas discharge display a... method for producing such a display.

The application is directed to a gas discharge display and a method for producing such a display, having first and second substrates of transparent material in which at least one of the substrates has at least one cavity and luminescent gas discharge material is placed in the cavity; the first and second substrates are wafer bonded together such that the substrates are joined together at all points of contact.

Emissive, large area displays are expected to have applications in the large flat panel television market, particularly for high definition television. Plasma displays are promising candidates for this application. Plasma displays are constructed by patterning orthogonal electrodes on glass substrates, placing spacers between the glass substrates, sealing the substrates at the periphery and filling the space in between the substrates with the working gas. In another version of a plasma panel, a glass sheet with holes cut through it is placed between electrode substrates. As a result, individual discharges are confined to the holes in the middle sheet. However, the seal is still made at the periphery and the gas is filled from a small opening at the periphery, which is thereafter sealed.

Since the conventional displays are large, the gas fill pressure cannot be much more than one atmosphere, as the forces on the glass substrate are too great and will either force the substrates apart, or shatter them. For example, in a panel measuring 1200 sq in (30x40 in), only 0.1 psi of pressure over 1 atmosphere will result in an outward force of 120 lbs on each substrate. Therefore, the gas fill in these substrates must be restricted to a maximum pressure of 1 atm.. At the same time, one of the key problems plaguing the plasma panels is low brightness for TV applications because of the lower pressure at which they must be operated.

This application is directed to a display technology based on micromachining, that will yield bright, efficient and rugged displays for TV applications. In this construction, the individual pixels may be completely isolated from each other. The individual pixels are formed by etching and bonding of the transparent substrates (glass, fused quartz, sapphire, PCA or others), so that the pixels are comprised of sealed cavities containing electrodes and the ambient gas or dosing material. Since in this particular case each pixel is a sealed cavity, which is formed by bonding the etched substrates, the bonded

interface is as strong as the bulk of the substrate and the pressure within such a pixel can be substantially more than one atmosphere.

The term "bonding" as used herein especially refers to "wafer bonding" techniques used in the manufacture of integrated circuits and sensors. Such techniques generally comprise anodic or fusion bonding which results in a chemical bond at the interface which is as strong as the bulk material. This bond permits the fabrication of cavities which can withstand extremely high pressures (greater than 200 atmospheres). In this technique, a bond is present at all points of contact between the substrate surfaces. So that each cavity is individually sealed.

There are two types of wafer bonding processes. Anodic wafer bonding or fusion wafer bonding. Fusion wafer bonding: In this process two flat wafers (e.g. quartz) are prepared with hydrophillic surfaces and brought into contact. The Van de Waal's forces pull the two wafers together and result in a bond at the interface. The two wafers are then annealed at high temperature (e.g. 1000 C), resulting in a chemical bond at the interface, which has the strength of the bulk material. Even though the temperature is elevated, bonding takes place at a temperature below the melting point of the material (quartz: approximately 1400°C). This means that the substrate will not deform during the bonding process. Anodic wafer bonding: In this process, two flat wafers are brought into contact as in the fusion wafer bonding process. However, the annealing is carried out at lower temperatures and with an electric field applied across the wafers. This process is useful for materials that have mobile ions and cannot be annealed at high temperatures (such as glass). The electric field results in the collection of positive and negative charges at the interface, which lead to high electric fields, which pull the wafers together. This process is more forgiving of the degree of wafer flatness, but is more difficult to implement and does not work with materials that are free of mobile ions.

The wafer bonding process can be used with IC techniques to make extremely small individually sealed cavities (<100 micron diameter) and is a batch process which is fully compatible with IC techniques. The present development also permits the phosphors that fluoresce to be located either inside the discharge cavity or outside of the cavity.

U.S. Patent No. 4,990,826 is directed to a display device. In this patent, channels are formed by etching through one plate and placing it in contact with two plates on which electrodes have been formed. The three plates are then sealed together by heating.

around the metal electrode and form a seal. Such heating may unacceptably deform the entire structure. In U.S. Patent No. 4,990,826, a vacuum port is also sealed into the device with glass frit. The discharge space is evacuated and filled through this port and then sealed by melting the pumping port tube.

The discharge space in the present invention is formed by bonding two or more plates together, especially waferbonding. The electrodes are sealed and the surface of the wafer is planarized by using wafer planarizing methods to deposit glass or SiO_2 films. The planarized wafers are then bonded together to seal the discharge space. Since the wafer bonding is carried out in the atmosphere required in the discharge space (e.g. Ar, Ne, Xe, etc.), the atmosphere is sealed into the cavity and a port is not required. Therefore, the present process allows the formation of many individually sealed cavities on one substrate, whereas the process described in U.S. Patent No. 4,990,826 does not. The present process has the advantages of batch processing whereas the prior art does not. The formation of a seal by wafer bonding also has practical advantages over glass softening, in that the structure will not deform during wafer bonding but will during softening of the glass as in U.S. Patent No. 4,990,826.

The improved construction can readily provide higher pressure discharges, which can emit substantially more light. This is particularly advantageous for HDTV applications, where pixel sizes need to be small ($<300\ \mu m$), even for large area displays. However, it is difficult to use mechanical processes economically to make small but deep apertures. Furthermore dry chemical etching processes are too slow and also too expensive. Therefore, the pixel cavities are made preferably by wet chemical etching, which is isotropic and results in etched cavities whose lateral dimensions are roughly twice the depth. Therefore, the spacing between electrodes must be kept small. However, in order to optimize the UV radiation from xenon, it has been demonstrated that the ratio of electric field to pressure (E/p) is 7-8V/cm.torr. Therefore, for driving voltages of 60V and electrode spacings less than 100 μm, the optimum pressure is more than one atmosphere which is not obtainable with prior manufacturing processes.

Although, the discussion so far has assumed that the discharges are in the "glow" phase, another advantage of this technology is that the pixels can be operated as high pressure arc lamps. It is well known that these high pressure arc lamps have significant output in the visible. Therefore, the pixels can be used with colour filters to form a display, thus avoiding the use of phosphors. When the discharge is operated in the "glow" phase, the electrodes do not get very hot, however, when the discharge is operated in the "arc" phase,

the electrodes get hot, thus the choice of the metal for the electrodes is a function of the desired operating range. Additionally, in the arc phase, re-ignition is a problem, but it can be avoided by use of an auxiliary discharge, which is hidden from view, but connected to the display discharge space as was done in prior panels.

For better understanding of the invention, reference is made to the following drawings which are to be taken in conjunction with the detailed description to follow:

Figures 1a-1d illustrate a first construction for a gas discharge display panel in accordance with the present invention;

Figures 2a-2d illustrate a second construction of a gas discharge display panel; and

Figures 3a-3e illustrate a third type of gas discharge display panel in accordance with the invention.

Figs. 1a-1d illustrate a first construction for a flat panel gas discharge display in accordance with the invention. The display construction begins with a first translucent or transparent substrate 200 upon which a series of metal first electrodes 202 are deposited and which extend across what will be the surface area of the display. First electrodes 202 are patterned and deposited by known metal deposition techniques, i.e. masking, etching and deposition of materials. The choice of the metal to be used in first electrodes 202 is determined by the operating conditions of the discharge and first electrodes 202 can be deposited by thick or thin film techniques. Thereafter, the surface of substrate 200 and first electrodes 202 is planarized by using planarizing techniques such as spin-on glass or the deposition of a phosphorous doped SiO_2 (p-glass) 204 followed by an annealing step to harden same. The substrate, metal first electrodes 202 and planarizing layer 204 are shown in Figure 1b.

Substrate 200 is then bonded to an intermediate substrate 206 in which a series of cavities (holes) 208 have been etched (or otherwise produced in) with the same spacing as that of electrodes 202 (see Fig. 1c). The sidewalls of the etched cavities 208 may be deposited with a phosphor 210, or other luminescent material if required by the display. The bonding of substrate 200 to perforated substrate 206 is accomplished by wafer bonding techniques such as fusion bonding or anodic bonding (as described above). The wafer bonding of substrates 200, 206 will join them together at all points of contract, other than at holes 208. After bonding of substrate 200 to substrate 206, the planarizing layer 204 is removed in the area of cavities 208 over first electrodes 202 which will expose electrodes

202 in cavities 208 of the display. The planarizing layer 204 can be removed in cavities 208 by the usual masking and etching techniques using photolithography or it could be left unremoved with a discharge formed by capacitive coupling.

Thereafter a third substrate 212 is prepared (Fig. 1c). Patterned and deposited on substrate 212 are a second pattern of metal electrodes 214 which in the final form will extend perpendicularly (orthogonally) to first electrodes 202. Substrate 212 is thereafter planarized with a planarizing layer 216. A masking and etching step is then used to remove the planarizing layer 216 in the areas that will be within discharge cavities 208. Finally, substrate 212 is wafer bonded to substrate 206 (which is already bonded to substrate 200), to form the finished display. This final bonding is carried about in the ambient atmosphere which is to be sealed into the individual cavities (i.e., argon, xenon, neon and/or helium for a plasma display). Any other necessary dosing material can also be placed in cavities 208 prior to forming the final wafer bond. As is shown in Figure 1d (which is a plan view of the finished assembly), the assembly consists a plurality of cavities 208 disposed within the display with the electrodes 202, 214 running perpendicular to each other and intersecting at cavities 208 (pixels). The width of electrodes 202, 214 is exaggerated so as to illustrate the construction. In practice, electrodes 202, 204 need not be as wide so as to not obscure the light emitted by individual cavities 208 (pixels). The three substrates may be formed by any suitable material such as glass, with quartz or sapphire utilized if the type of discharge requires it.

Figure 2a - 2d illustrate a second construction for a gas discharge display in accordance with the present invention. This construction differs from that of Figure 1 in that the need for depositing planarizing layers is eliminated. As shown in Figure 2, a first substrate 220 is etched with a series of trenches 222 in which are deposited first electrodes 224 as shown in Fig. 2b. Thereafter, substrate 220 is wafer bonded to a perforated second substrate 226. Second substrate 226 contains a multiplicity of cavities 228 which will form the individual picture elements (pixels) of the display. The spacing between cavities 228 is the same as between electrodes 224.

Third substrate 230 is prepared in the same manner as substrate 220, that is a series of trenches 232 are etched therein and second electrodes 236 are deposited therein. Substrate 230 is wafer bonded to the upper portion of substrate 226 and is arranged so that first electrodes 224 are disposed orthogonally with respect to second electrodes 236. Since the electrodes 224 and 236 are disposed in trenches, a proper sealing of cavities 228 is not accomplished by the wafer bonding of the three substrates together. The sealing of cavities

228 is accomplished by means of a CO_2 laser. As is seen in Figure 2d laser seals 238, 240 seal electrodes 224 to substrate 220 while laser seals 242, 244 are utilized to seal electrodes 236. The laser will melt and fuse the material of the substrates around the electrodes to seal each of the cavities. The laser is applied in the ambient atmosphere that is to be sealed within the cavities. The laser beam can be sharply focused so that the melting of the substrate material takes place only at the aim points of the laser beam and does not affect the integrity of the display as a whole.

Figure 3a - 3e illustrates yet another construction for a gas plasma display which utilizes two, rather than three, substrates and which disposes the electrodes along the side of the discharge cavities to minimize obstruction. In this construction, a first substrate 300 is patterned and etched with a series of trenches 302 in which a series of metal first electrodes 304 are deposited. As seen in the plan view of Figure 3e, electrodes 304 have extensions 310 extending laterally there from. A planarizing layer 306 is then deposited over substrate 300 and electrodes 304. Thereafter polysilicon masks 308 are deposited over the planarizing layer 306. As shown in Figure 3b, polysilicon masks 308 extend only partially over extensions 310 of electrodes 304. As shown in Figure 3c, half cavities 312 are then etched with the polysilicon masks 308 preventing etching thereunder. The etchant used is one which will etch the material of substrate 300 and planarizing layer 306 but does not substantially affect electrode 304. As shown in Figure 3c after the etching process and the removal of the polysilicon, electrode extensions 310 extend into individual half cavities 312.

As illustrated in Figure 3c, the finished substrate 300 has an upper surface which is planar, which permits direct bonding to a second substrate. As shown in Figure 3d, a second substrate 320 is prepared in a similar manner to that of substrate 300 in that it is etched with a series of trenches 322 and deposited with second electrodes 324 which have a L-shaped extension 326 (see Fig. 3e). Thereafter, a planarizing layer 328 is deposited over electrodes 324 and a polysilicon mask (not shown) is applied which is used to mask the etching of second half cavities 330 in the same manner as described above with respect to substrate 300. After preparation of substrate 320, substrate 300 is wafer bonded to substrate 320 to form the finished sealed cavities as shown in Figure 3d. As is seen in the top view of Figure 3e, a plurality of cavities are formed which have electrodes extending laterally thereinto. It is seen that in this view, the electrodes obscure very little of the individual cavities which permits greater brightness from the resulting matrix of pixels forming the display. This construction makes use of planarizing layers, however it is to be noted that the planarizing layers could be omitted and the cavities sealed by laser application as described

above with respect to the display of Fig. 2.

As is seen, the completed panels have upper and lower electrodes arranged orthogonally with respect to each other, i.e. in a row and column arrangement. This arrangement permits each discharge cavity (pixel) to be individually activated (addressed) thus these displays can be used for information or video display purposes. Since each cavity can be individually doped prior to final sealing, appropriate dopants to create various colours or three colours (red, green and blue) for full colour displays may be utilized with this technology. Since the cavities will easily contain high pressures greater brightness can be achieved.

The above described structures and methodology are merely illustrative of the principles of the present invention. Numerous modifications and adaptations thereof will be readily apparent to those skilled in the art without departing from the spirit and scope of the present invention and the appended claims. In particular the cavities need not be completely isolated.

CLAIMS:

1. A gas discharge display having first and second substrates of transparent material, a plurality of cavities disposed between said substrates, a plurality of first and second electrodes disposed within said cavities; and luminescent gas discharge material disposed in said cavities, said first and second substrates being wafer bonded together at all points of contact.

2. The gas discharge display as claimed in Claim 1, wherein said first and second electrodes are disposed orthogonally with respect to each other.

3. The display as claimed in Claim 2, further including a third substrate, disposed between said first and second substrates in which said cavities are disposed.

4. The display as claimed in Claim 1, wherein said cavities are provided by half cavities in each of said substrates.

5. The gas discharge display as claimed in Claims 1-4, characterized in that a phosphor is disposed within said cavities.

6. A method for fabricating a gas discharge display having the steps of: providing a first and second substrate of transparent material, providing a plurality of cavities in at least one of said substrates, filling the cavities with gas discharge material that will luminesce when activated, providing first and second electrodes on at least one of said substrates and bonding said first and second substrates together at all points of surface contact between the substrates to seal said cavity.

7. The method as claimed in Claim 6, further including the step of bonding an intermediate substrate between said first and second cavities.

8. The method as claimed in Claim 7, further including the step of planarizing the surface of said substrate prior to said bonding.

9. The method as claimed in Claim 6, further including the step of applying laser radiation so as to seal said electrodes to said substrates.

10. The method as claimed in Claim 6, further including the step of etching channels in the surface of said substrates and depositing said electrodes in said channels.

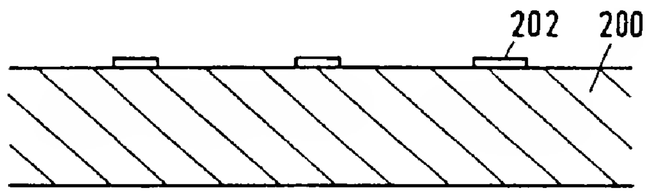

FIG.1a

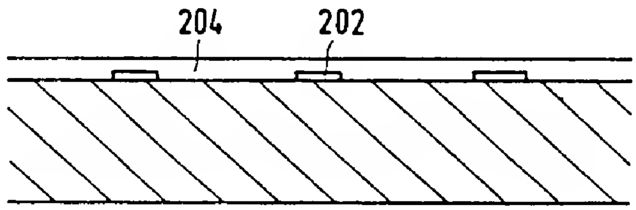

FIG.1b

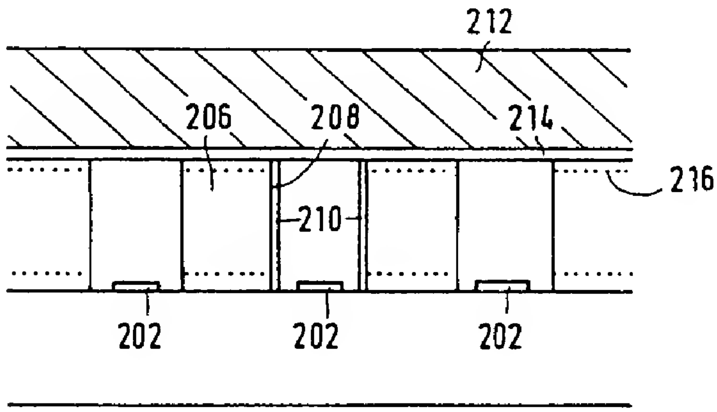

FIG.1c

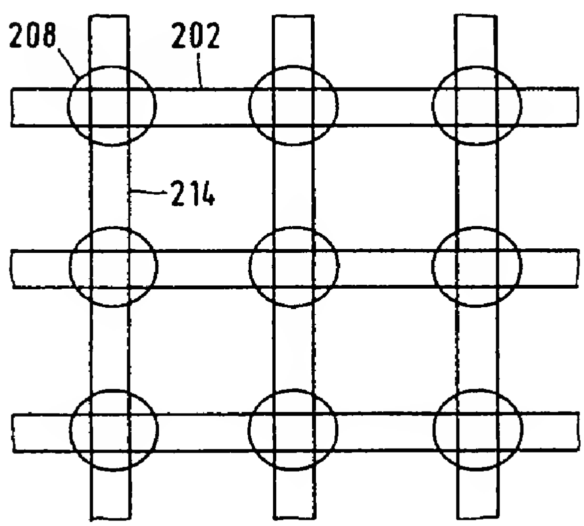

FIG.1d

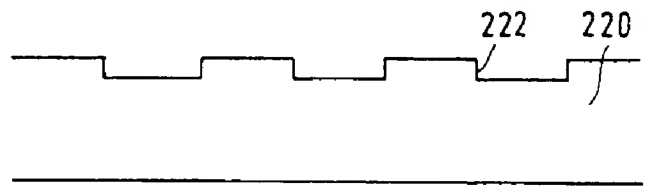

FIG.2a

FIG.2b

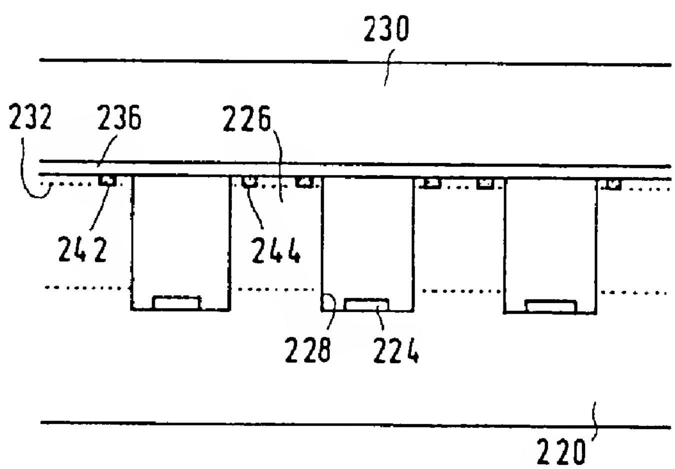

FIG.2c

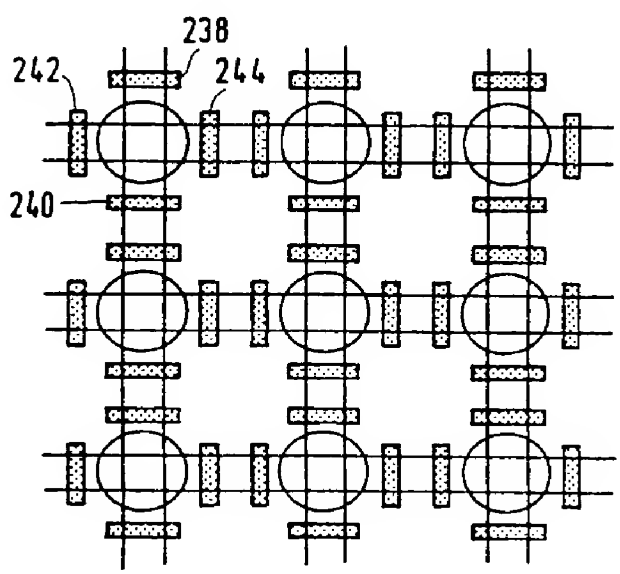

FIG.2d

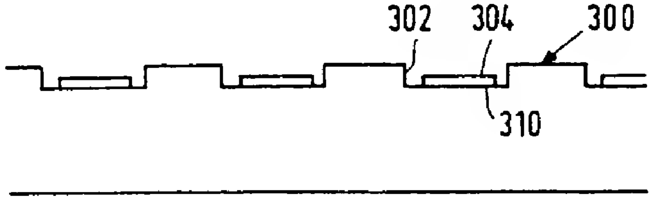

FIG.3a

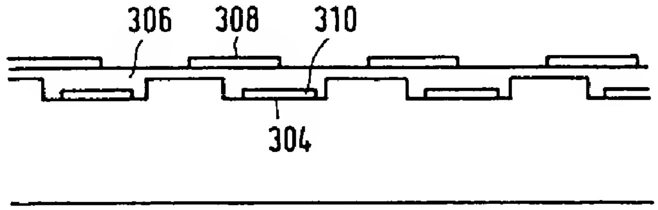

FIG.3b

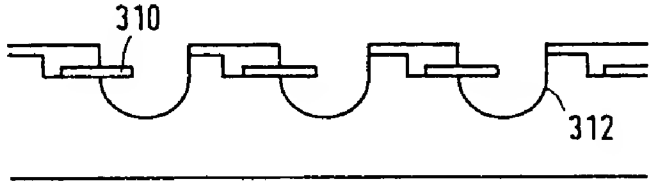

FIG.3c

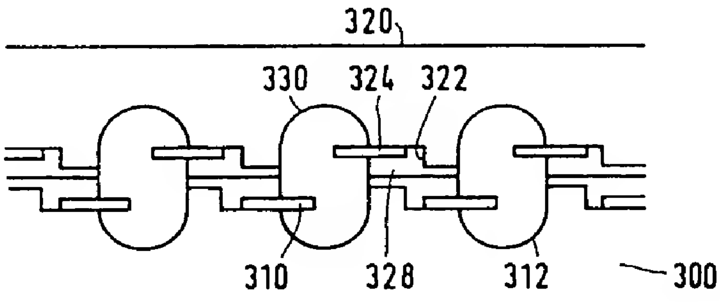

FIG.3d

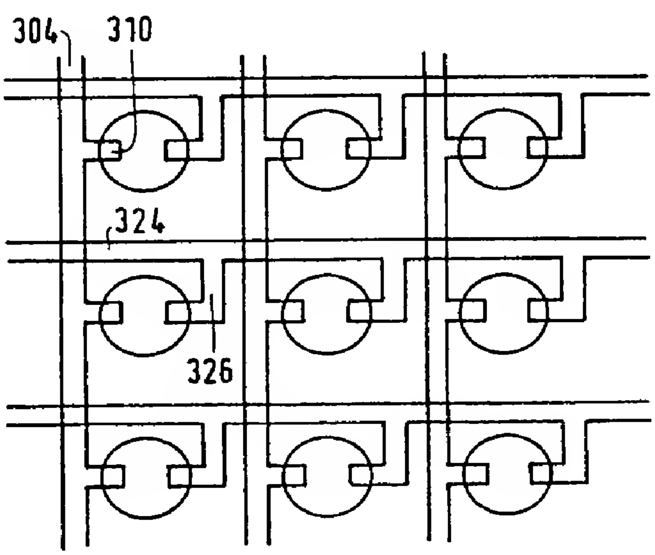

FIG.3e